SIS3400 CDMS II
VME TDC/Time Stamper

User Manual

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Revision	Date	Modification
0.1	26.10.00	Generation from SIS3400
1.0	31.10.00	First official release
1.01	07.11.00	Missing registers added, several additions
1.02	12.01.01	Experiment name fix -> CDMSII
1.03	15.01.01	Add missing control bits, add getting started table
1.10	22.05.01	Firmware version 0xA, FIFO word counter time counter reset upon global reset
1.20	20.03.02	Firmware version 0xB TIME_STAMP expanded to 32 bits

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2 Introduction

The SIS3400 is a versatile 64 channel TTL or RS485 (CDMS II version) input module. The card is a single width 6U VME board with hard metric coaxial input connectors. Possible applications of the board comprise standard multi event latch, self triggering latch, trigger time stamp generator and TDC for low speed applications.

Initially the development of the card was driven by the requirements of users from the Neutron Scattering community in the context of the readout of a large scale Time Of Flight (TOF) spectrometer at the Garching FRM II research reactor. As in the order of 14 front end modules will be in use over a long time scale, design aspects like ease of maintenance and minimum overhead system integration played an important role. The result are features like hot swap and geographical addressing. To follow VMEs tradition of downward compatibility cstandard VME addressing is implemented as well.

This manual describes the SIS3400 version, which was developed for the CDMS II experiment, the main changes are SCSI style 68 pin input connectors in conjunction with LEMO control connectors and RS485 level compatible receivers (TTL in the control case) and a dedicated firmware design.

As we are aware, that no manual is perfect, we appreciate your feedback and will try to incorporate proposed changes and corrections as quickly as possible. The most recent version of this manual can be obtained by email from info@struck.de, the revision dates are online under http://www.struck.de/manuals.htm. A list of available firmware designs can be retrieved from http://www.struck.de/sis3400firm.htm

3 Technical Properties/Features

Find below a list of key features of the SIS3400 CDMSII.

- 64 channels
- 3 control in- and 3 control outputs
- 32-bit time bin counter with wrap around counter
- TTL level for control signals
- RS485 input level
- SCSI style 68-pin input connectors
- Derandomiser FIFO
- Output FIFO
- Leading Edge (input inversion through control register)
- FIFO and wrap around interrupts
- external/internal clock
- external/internal software inhibit
- software time reset/zero
- Up to four firmware files
- A24/32 D32/BLT32/MBLT64Geographical addressing mode (in conjunction with VME64x backplane)
- Hot swap (in conjunction with VME64x backplane)
- VME64x Connectors
- VME64x Side Shielding
- VME64x Front panel
- VME64x extractor handles (on request)
- single supply (+5 V)

3.1 Board Design

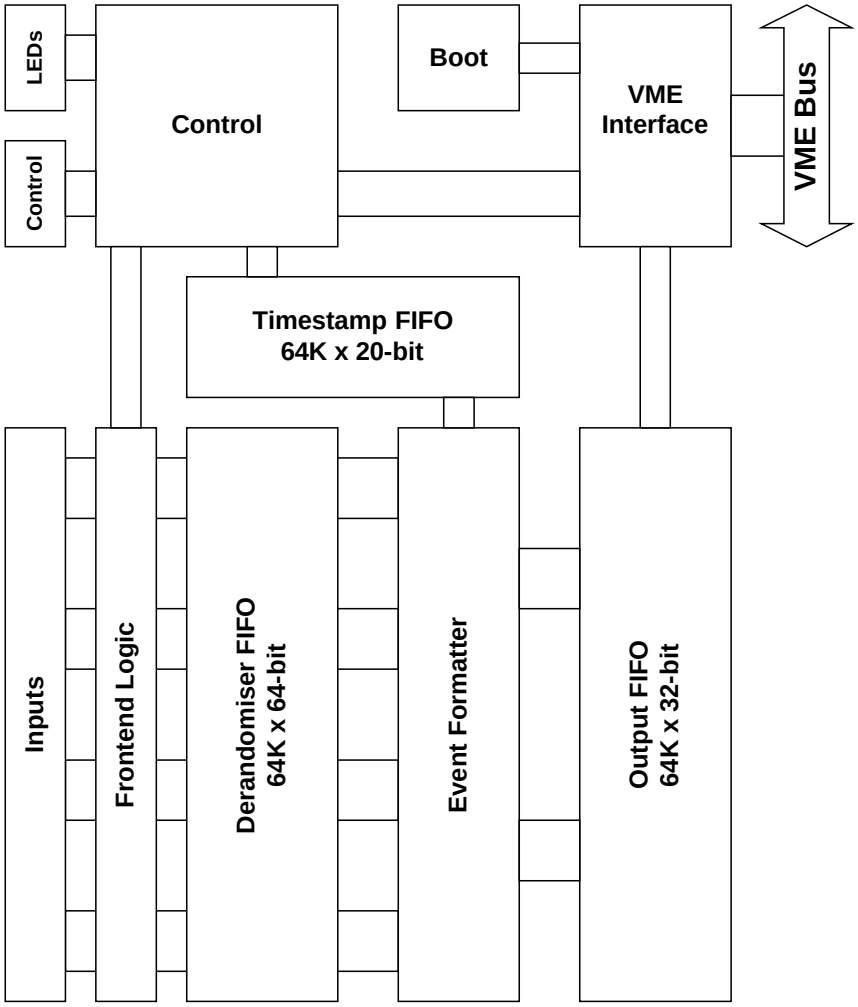
As can be seen in the block diagram below, the SIS3400 is implemented as a two stage FPGA-FIFO (Field Programmable Gate Array-First In First Out memory) design. The 64 input channels are connected to the three first stage FPGAs through input drivers. Depending on the decision of the input stage FPGAs the 64-bit word and possibly additional information like the event time stamp is stored in the input FIFO group (which consists of 5 18-bit x 64K FIFO chips). The so called event formatter FPGA processes data from the input FIFOs and stores the result in the output FIFOs. (the output FIFO group consists of 2 18-bit x 64K FIFO chips) as long as the availability of sufficient space for the event is insured. Event processing pauses as long as the FIFO almost full condition if flagged by the output FIFOs. If the VME CPU side can not cope with the output data rate the input FIFO stage will finally reach the almost full condition as well and the Veto output will be set.

Note:
the sustained input data rate of the input FPGAs of a SIS3400 which is clocked at **10 MHz** (100 ns time bins) is 80 Mbyte/s (8 byte x 10 MHz).

3.2 SIS3400 CDMS II input stage firmware

The SIS3400 CDMS II input stage firmware is edge sensitive. Input channels with a leading edge within the time slice (clock cycle) will have their corresponding bit set in the input data word. To allow for maximum flexibility the inputs can be inverted in the input stage FPGAs via the two input stage inversion registers .
Data words with one or more leading edges will be stored in the input FIFO stage with the corresponding counter value written to the time stamp FIFO upon the next leading edge of the clock. While single wire and event mode are still available as formatter data handling options, it is obvious, that no leading/trailing edge recognition is available. The formatter processing time depends on the selected mode of operation. In multi wire mode it is in the order of 1 µs, in single wire it is in the order of 5 µs. This value can be regarded as conversion time in combination with the clock period. A module operated in event mode at a clock period of 1 µs will have the event data stored in the output FIFO after some 2 µs. .

Note: Set Bits in the input stage Xilinx chips are cleared with the leading edge of the next clock tick. During this process, which takes approximately 25 ns, a new leading edge may not be detected, i.e. the safe double pulse resolution is clock + 25 ns.

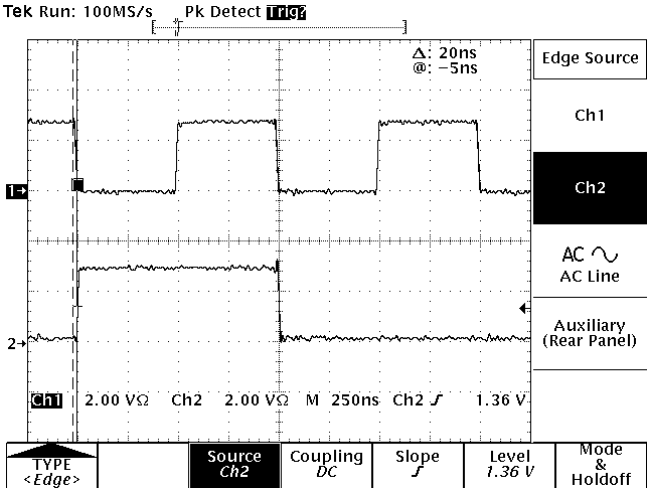


SIS3400 Block Diagram

3.2.1 Clock Synchroniser/Clock receiver

The first SIS3400 CDMSII in a multi module setup acts as the clock synchroniser, following modules in the clock chain act as clock receiver modules. The power up default setting is implemented in a fashion, that the unit will power up as clock synchroniser, what is the proper setting for a single board. The clock synchroniser will synchronise start and stop signals (via front panel or VME) to the negative edge of the clock and the positive clock edge will be used to latch the data on the clock receiver modules to guarantee for synchronisation of all modules in the chain. Starts and stops (by front panel as well as by VME) are synchronised to the clock as shown in the scope shot below, the outgoing start/stop pulse has a width of one clock period.

Note: The user has to make sure to provide a symmetric external clock (the internal 1 MHz clock is symmetric)



The scope shot above shows the clock on the upper trace and the synchronised start/stop pulse on the lower trace

4 Getting Started

The minimum setup to operate the SIS3400 CDMSII requires the following steps:

- Select the proper boot mode and firmware design with jumper J34
- Select the VME addressing mode with jumper J1
- Set the base address (if a non geographical addressing mode is used) with SW1 and SW2
- turn VME crate power off
- install the module in the VME crate
- turn crate power back on
- issue a key reset
- define clock receiver (if not first module in the chain)
- define clock source (1 MHz internal, 20 MHz internal, external or VME key)
- select input inversion inputs 64:33 and 32:1 (if required)
- select control input inversion (if required, see section 6)
- enable front panel control inputs
- select formatter mode (single wire e.g.)
- set formatter module address if desired
- enable input control logic (starts counter, arms for start/stop)

A good way of checking first time communication with the SIS3400 consists of switching on the user LED by a write to the control register at offset address 0x0 with data word 0x1 (the LED can be switched back off by writing 0x100 to the control register).

Getting started address/bit table:

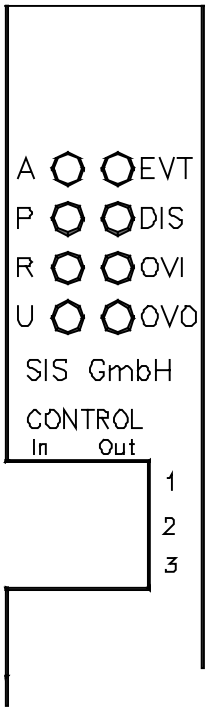
Function	Address offset	Datum to write
Key reset	0x20	arbitrary
Define clock receiver (omit for first module in chain)	0x0	0x40
Define clock source (omit for front panel clock or VME key))	0x0	0x8 (1 MHz) 0x4 (10 MHz)
Select input inversion inputs 64:33 (if required)	0x204	0x1
Select input inversion inputs 32 (if required)	0x304	0x1
Select control input inversion (if required)	0x0	0x50
Enable front panel control inputs (ored with VME control)	0x0	0x10
Select formatter mode (select single wire mode, omit for multi wire mode)	0x100	0x1
Set formatter module address (omit if 0 is fine with you)	0x104	0x0-0x1F
Enable input control logic	0x28	arbitrary

5 Front Panel LEDs

The SIS3400 has 8 front panel LEDs to visualise part of the units status. Three LEDs according to the VME64xP standard (Power, Access and Ready) plus 5 additional LEDs (VME user LED, EVT, DIS, OVI and OVO LED).

Designation	LED	Color	Function
A	Access	yellow	Signals VME access to the unit
P	Power	red	Flags presence of VME power
R	Ready	green	Signals configured logic
U	VME user LED	green	To be switched on/off under user program control
EVT	Event	yellow	Signals one or more leading edges in time slice (i.e. data word is copied to input FIFO)
DIS	Disable	red	Signals disabled or no gate present state
OVI	Overflow Input	green	Signals input FIFO overflow
OVO	Overflow Output	green	Signals output FIFO overflow

The LED locations are shown in the portion of the front panel drawing below.



The VME Access and the EVT LED are monostable (i.e. the duration of the on phase is stretched for better visibility), the other LEDs reflect the current status.
An LED test cycle is performed upon power up (refer to chapter 15.1).

6 Front Panel Control In/Outputs

Six control signals are implemented in the SIS3400 CDMSII design, three inputs and three outputs. Their location can be seen on the drawing above.

Input	Output	
Clock	Clock	1
Start	Start	2
Stop	Stop	3

The input to output delay is approx. 15 ns.

Note: The internal clock will not be "seen" by the module if front panel input is enabled and the external clock input is high (open and terminated with 4,7 KΩ to V_{CC} e.g.). I.e. the internal and external clock signals are ored). See section 8.2 for control input inversion

7 VME addressing

7.1 Address Space

Depending on the selected addressing mode the module occupies 16-bits (A24 mode) or 24-bits (A32 mode) of the VME addressing space.

7.2 Base Address

7.2.1 VME

Besides standard A24 and A32 addressing the SIS3400 offers a pragmatic geographical addressing mode. VIPA geographical addressing is foreseen as a possible future option, but was considered too complex for the Neutron TOF application. The base address is defined by the selected addressing mode, which is defined by jumper array J1 and possibly SW1 and SW2 (in non geographical mode).

The table below summarises the possible base address settings.

set jumper(s) of J1				Address Bits															
A32	A24	GEO	VIPA	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
x				SW2				SW1				0				0			x
	x			not decoded				not decoded				SW2				SW1			
x		x		0	0	0	GA4	GA3	GA2	GA1	GA0	0	0	0	0	0	0	0	x
	x	x		not decoded				not decoded				0	0	0	GA4	GA3	GA2	GA1	GA0
			x	not implemented in current firmware															

Shorthand	Explanation
SW1/SW2	Setting of rotary switch SW1 or SW2 respective
GA0-GA4	Geographical address bit as defined by the VME64x(P) backplane

The factory default setting for the SIS3400 CDMSII is shipped with SW2 set to 3 and SW1 set to 4 and A32 and A24 enabled, hence the module will respond to A32 0x34000000 and A24 0x340000.

7.3 Address Map

The SIS3400 board is operated via VME registers and VME key address cycles, output data are read from the FIFO. The following table gives an overview on all SIS3400 addresses and their offset from the base address, a closer description of the registers and their function is given in the following subsections.

Note: Write access to a key address (KA)with arbitrary data invokes the respective action

Offset	Key	Access	Type	Function
0x000		R/W	D32	Control and Status register
0x004		R/W	D32	Module Identification and IRQ control register
0x020	KA	W	D32	Global Reset (like Power On) clear time counter also (from firmware rev. 0xA on)
0x028	KA	W	D32	Enable INPUT Control Logic
0x02C	KA	W	D32	Disable INPUT Control Logic
0x030	KA	W	D32	Start (start of gate)
0x034	KA	W	D32	Stop (end of gate)
0x038	KA	W	D32	INPUT Control CLOCK pulse
0x03C	KA	W	D32	INPUT Control CLEAR pulse (clears time counter)
Formatter				
0x100		R/W	D32	Formatter Control/Status register
0x104		R/W	D32	Formatter Module Address register (module number)
0x108		R	D32	FIFO Flag Status register
0x10C		R/W	D32	FIFO Flag IRQ Enable control register
0x110		R/W	D32	Upper Test register for Output FIFO Test ;data bits [31:16]
0x114		R/W	D32	Lower Test register for Output FIFO Test ;data bits [15:0]
0x118		R	D32	Output FIFO word counter
0x120	KA	W	D32	Write test data into Output FIFO (if Test is enabled)
0x130	KA	W	D32	Clear all FIFOs and FIFO word counter

Input1 64-33				
0x200		R/W	D32	Input group 1 Control/Status register
0x204		R/W	D32	Input inversion channel 63:32 Bit0=0 non inverting, Bit0=1 inverting
0x210		R/W	D32	Test register 1 for Input FIFO Test; input data [64:57]
0x214		R/W	D32	Test register 2 for Input FIFO Test; input data [56:49]
0x218		R/W	D32	Test register 3 for Input FIFO Test; input data [48:41]
0x21C		R/W	D32	Test register 4 for Input FIFO Test; input data [40:33]
0x220		R	D32	Input Buffer 1 ; input data [64:57]
0x224		R	D32	Input Buffer 2 ; input data [56:49]
0x228		R	D32	Input Buffer 3 ; input data [48:41]
0x22C		R	D32	Input Buffer 4 ; input data [40:33]
0x230		R	D32	Time Shadow Register 1; Bits [64:57]
0x234		R	D32	Time Shadow Register 2; Bits [56:49]
0x238		R	D32	Time Shadow Register 3; Bits [48:41]
0x23C		R	D32	Time Shadow Register 4; Bits [40:33]
Input2 32-1				
0x304		R/W	D32	Input inversion channel 32:1 Bit0=0 non inverting, Bit0=1 inverting
0x310		R/W	D32	Test register 5 for Input FIFO Test; input data [32:25]
0x314		R/W	D32	Test register 6 for Input FIFO Test; input data [24:17]
0x318		R/W	D32	Test register 7 for Input FIFO Test; input data [16:9]
0x31C		R/W	D32	Test register 8 for Input FIFO Test; input data [8:1]
0x320		R	D32	Input Buffer 5 ; input data [32:25]
0x324		R	D32	Input Buffer 6 ; input data [24:17]
0x328		R	D32	Input Buffer 7 ; input data [16:9]
0x32C		R	D32	Input Buffer 8 ; input data [8:1]
0x8000 to 0xFFFC		R	D32/ BLT32/ MBLT64	Output FIFO on A24 access
0x10000 to 0x1FFFC		R	D32/ BLT32/ MBLT64	Output FIFO on A32 access

Note: D08 and D16 are not supported by the SIS3400 board

8 Register Description

8.1 Status Register (0x0)

The status register reflects the current settings of most of the SIS3400 parameters in read access, in write access it functions as the control register.

Bit	Function
31	0
30	Status VME IRQ source 2 (test IRQ)
29	Status VME IRQ source 1 (ext. clock shadow)
28	Status VME IRQ source 0 (Overflow)
27	VME IRQ
26	internal VME IRQ
25	0
24	0
23	Status reserved 15
22	Status VME IRQ Enable Bit Source 2
21	Status VME IRQ Enable Bit Source 1
20	Status VME IRQ Enable Bit Source 0
19	Status reserved 11
18	Status reserved 10
17	Status reserved 9
16	Status reserved 8
15	Global INPUT Control Logic Enable bit
14	Gate (reflects current gate status)
13	0
12	0
11	0
10	0
9	0
8	0
7	Status input test
6	Status clock synchroniser
5	Status front panel input inversion
4	Status front panel control input
3	Status Enable 1 MHz CLOCK
2	Status Enable 10 MHz CLOCK
1	Status IRQ source 2 for software IRQ testing
0	Status user LED

The power up or key reset content is 0x0 (see default settings of control register).

8.2 Control Register (0x0)

The control register is in charge of the control of most of the basic properties of the SIS3400 board in write access. It is implemented via a selective J/K register, a specific function is enabled by writing a 1 into the set/enable bit, the function is disabled by writing a 1 into the clear/disable bit (which has a different location within the register). An undefined toggle status will result from setting both the enable and disable bits for a specific function at the same time.
On read access the same register represents the status register.

Bit	Function
31	clear reserved 15 (*)
30	disable IRQ source 2 (*)
29	disable IRQ source 1 (*)
28	disable IRQ source 0 (*)
27	clear reserved 11 (*)
26	clear reserved 10 (*)
25	clear reserved 9 (*)
24	clear reserved 8 (*)
23	set reserved 15
22	enable IRQ source 2 (test)
21	enable IRQ source 1 (input; counter IRQ; Counter overflow (toggle bit 20))
20	enable IRQ source 0 (formatter)
19	set reserved 11
18	set reserved 10
17	set reserved 9
16	set reserved 8
15	Disable input test (*)
14	Enable clock master (*)
13	Disable control input inversion (*)
12	Disable front panel control inputs (*)
11	Disable 1 MHz CLOCK (*)
10	Disable 10 MHz CLOCK (*)
9	clear IRQ test (source 2) (*)
8	switch off user LED (*)
7	Enable input test
6	Disable clock master
5	Enable control input inversion
4	Enable front panel control inputs
3	Enable 1 MHz CLOCK
2	Enable 10 MHz CLOCK
1	set IRQ test (source 2)
0	switch on user LED

(*) denotes the default power up or key reset state

8.3 Module Identification and IRQ control register (0x4)

This register has two basic functions. The first is to give information on the active firmware design. This function is implemented via the read only upper 20 bits of the register. Bits 16-31 hold the four digits of the SIS module number (like 3400 e.g.), bits 12-15 hold the version number. The version number allows a distinction between different implementations of the same module number, the SIS3400 for example has the frontend module mode and the clock module mode as versions.
Control register bit assignment table:

Bit	Read/Write access	Function	
31	read only	Module Identification Bit 15	Module Id Digit 3
30	read only	Module Identification Bit 14	
29	read only	Module Identification Bit 13	
28	read only	Module Identification Bit 12	
27	Read only	Module Identification Bit 11	Module Id Digit 2
26	read only	Module Identification Bit 10	
25	read only	Module Identification Bit 9	
24	read only	Module Identification Bit 8	
23	read only	Module Identification Bit 7	Module Id Digit 1
22	read only	Module Identification Bit 6	
21	read only	Module Identification Bit 5	
20	read only	Module Identification Bit 4	
19	read only	Module Identification Bit 3	Module Id Digit 0
18	read only	Module Identification Bit 2	
17	read only	Module Identification Bit 1	
16	read only	Module Identification Bit 0	
15	read only	Version Bit 3	
14	read only	Version Bit 2	
13	read only	Version Bit 1	
12	read only	Version Bit 0	
11	read/write	VME IRQ Enable (0=IRQ disabled, 1=IRQ enabled)	
10	read/write	VME IRQ Level Bit 2	
9	read/write	VME IRQ Level Bit 1	
8	read/write	VME IRQ Level Bit 0	
7	read/write	IRQ Vector Bit 7; placed on D7 during VME IRQ ACK cycle	
6	read/write	IRQ Vector Bit 6; placed on D6 during VME IRQ ACK cycle	
5	read/write	IRQ Vector Bit 5; placed on D5 during VME IRQ ACK cycle	
4	read/write	IRQ Vector Bit 4; placed on D4 during VME IRQ ACK cycle	
3	read/write	IRQ Vector Bit 3; placed on D3 during VME IRQ ACK cycle	
2	read/write	IRQ Vector Bit 2; placed on D2 during VME IRQ ACK cycle	
1	read/write	IRQ Vector Bit 1; placed on D1 during VME IRQ ACK cycle	
0	read/write	IRQ Vector Bit 0; placed on D0 during VME IRQ ACK cycle	

The second function of the register is interrupt control. The interrupter type of the SIS3400 is D08(O) ROAK . Via bits 0-7 of the module identifier and interrupt control register you can define the interrupt vector, which is placed on the VME bus during the interrupt acknowledge cycle. Bits 8 through 10 define the VME interrupt level, bit 11 is used to enable (bit set to 1) or disable (bit set to 0) interrupting.

Module identification and version example:

The register for a SIS3400 CDMSII reads **0x3400Bnnn** (the status of the lower 3 nibbles is denoted with n in the example).

8.4 Formatter Control/Status Register (0x100)

The behaviour of the event formatter can be controlled through this register. On read access the register represents the formatter status register.

Bit	Read/Write access	Function
31	read only	No function ; read “0”
..	..	
..	..	
16	read only	No function ; read “0”
15	read/write	reserved
14	read/write	reserved
13	read/write	reserved
12	read/write	reserved
11	read/write	reserved
10	read/write	reserved
9	read/write	reserved
8	read/write	reserved
7	read/write	reserved
6	read/write	reserved
5	read/write	reserved
4	Read/write	OUTPUT_FIFO_TEST Mode
3	read/write	reserved
2	read/write	reserved
1	Read/write	reserved
0	Read/write	single wire mode (else multi wire mode if 0)

Power up default reading: 0x00000000

8.5 Formatter Module Address register (0x104)

This read/write register defines the address, which is copied into the output FIFO data stream of the SIS3400. In a multi module setup a detector channel is identified by its channel number (0-63) and its formatter module address (0-15), i.e. up to 1024 detector channels can be identified in a unique fashion without additional data to be added by the VME CPU.

Bit	Read/Write access	Function
31	read only	No function ; read “0”
..	..	
..	..	
8	read only	No function ; read “0”
7	read only	No function ; read “0”
6	read only	No function ; read “0”
5	read only	No function ; read “0”
4	read/write	Module Address Bit 4 (used in data stream)
3	read/write	Module Address Bit 3 (used in data stream)
2	read/write	Module Address Bit 2 (used in data stream)
1	read/write	Module Address Bit 1 (used in data stream)
0	read/write	Module Address Bit 0 (used in data stream)

The power up value of the register is: 0x00000000

8.6 FIFO Flag Register (0x108; read only)

The status of the input FIFO group and the output FIFO group can be retrieved from this read only register. In most cases the evaluation of the FIFO flag register of all frontend modules will be a good way to control overall readout. As an alternative the FIFO flags can be used to generate interrupts with the interrupt service routine handling readout.

Bit	Read Function
31	0
..	
..	
16	0
15	0
14	0
13	0
12	Input FIFO flag full
11	Input FIFO flag almost full
10	Input FIFO flag half full
9	Input FIFO flag almost empty
8	Input FIFO flag empty
7	0
6	0
5	0
4	Output FIFO flag full
3	Output FIFO flag almost full
2	Output FIFO flag half full
1	Output FIFO flag almost empty
0	Output FIFO flag empty

The reading of the status register after power up or key reset is 0x303

8.7 FIFO Flag IRQ Enable register (0x10C)

This read/write register defines which condition(s) of the output FIFO will generate an interrupt for interrupt driven readout applications. The optimum setting will depend on application, data rate and performance of the VME master.

Bit	Read/Write access	Function
31	read only	No function ; read “0”
..	..	
..	..	
16	read only	No function ; read “0”
15	read/write	reserved
14	read/write	reserved
13	read/write	reserved
12	read/write	reserved
11	read/write	reserved
10	read/write	reserved
9	read/write	reserved
8	Read/write	reserved
7	Read/write	reserved
6	Read/write	reserved
5	Read/write	reserved
4	Read/write	Enable IRQ if Output FIFO is full
3	Read/write	Enable IRQ if Output FIFO is almost full
2	Read/write	Enable IRQ if Output FIFO is half full
1	Read/write	Enable IRQ if Output FIFO is NOT almost empty
0	Read/write	Enable IRQ if Output FIFO is NOT empty

Power up default value: 0x00000000

8.8 Output FIFO test registers (0x110 and 0x114)

Data can be written to the 32-bit wide output FIFO through the upper and lower test register if output FIFO test mode is enabled. . To transfer the data of the two test registers to the FIFO a key address cycle to address 0x120 is required.

8.8.1 Upper Test register for Output FIFO Test (0x110)

Bit	Read/Write access	Function
31	Read only	No function ; read “0”
..	..	
..	..	
16	Read only	No function ; read “0”
15	Read/write	Output Fifo Test Data Bit 31
..	..	
..	..	
0	Read/write	Output Fifo Test Data Bit 16

Power up default value: 0x00000000

8.8.2 Lower Test register for Output FIFO Test (0x114)

Bit	Read/Write access	Function
31	read only	No function ; read “0”
..	..	
..	..	
16	read only	No function ; read “0”
15	read/write	Output Fifo Test Data Bit 15
..	..	
..	..	
0	read/write	Output Fifo Test Data Bit 0

after power up: 0x00000000

8.9 Output FIFO word counter (0x118)

The read only, 16-bit wide, output FIFO word counter is incremented with every word stored in the output FIFO. It is reset upon global reset (KA 0x20) or the clear all FIFO (KA 0x130) command.

8.10 Input group 1 Control/Status register (0x200)

The contents of the time shadow register can be frozen for readout by setting bit 0 of the input group control register to ensure, that no changes occur while the actual time value is read from time shadow registers 1 through 4.
Note: there is no equivalent group 2 register.

Bit	Read/Write access	Function
31	read only	No function; read as 0
..	..	
..	..	
8	read only	No function; read as 0
7	read/write	reserved, read as 0
6	read/write	reserved, read as 0
5	read/write	reserved, read as 0
4	read/write	reserved, read as 0
3	read/write	reserved, read as 0
2	read/write	reserved, read as 0
1	read/write	reserved, read as 0
0	read/write	TIME Shadow Register freeze bit

The power up reading is: 0x00000000

8.11 Input inversion group 1 register (0x204)

After power up the SIS3400 CDMS II latches leading edge transitions as “1”. Trailing edges can be selected for input channels 64 to 33 by setting bit 0 of this register.

Bit	Read/Write access	Function
31	read only	No function; read as 0
..	..	
..	..	
8	read only	No function; read as 0
7	read/write	reserved, read as 0
6	read/write	reserved, read as 0
5	read/write	reserved, read as 0
4	read/write	reserved, read as 0
3	read/write	reserved, read as 0
2	read/write	reserved, read as 0
1	read/write	reserved, read as 0
0	read/write	Input group 1 (channels 64:33) inversion mode

The power up reading is: 0x00000000

8.12 Input Group 1 FIFO test registers(0x210, 0x214, 0x218, 0x21C)

Data can be written to the input FIFO through the four input group1 FIFO test registers and the four input group 2 FIFO test registers. The data are copied to the input FIFO with a key address 0x38 access if input control mode 3 is avtive.

8.12.1 Test register 1 for Input FIFO Test (0x210)

Bit	Read/Write access	Function
31	Read only	No function ; read “0”
..	..	
..	..	
8	Read only	No function ; read “0”
7	Read/write	Input Fifo Test Data Bit 63
..	..	
..	..	
0	Read/write	Input Fifo Test Data Bit 56

after power up: 0x00000000

8.12.2 Test register 2 for Input FIFO Test (0x214)

Bit	Read/Write access	Function
31	Read only	No function ; read “0”
..	..	
..	..	
8	Read only	No function ; read “0”
7	Read/write	Input Fifo Test Data Bit 55
..	..	
..	..	
0	Read/write	Input Fifo Test Data Bit 48

after power up: 0x00000000

8.12.3 Test register 3 for Input FIFO Test (0x218)

Bit	Read/Write access	Function
31	Read only	No function ; read “0”
..	..	
..	..	
8	Read only	No function ; read “0”
7	Read/write	Input Fifo Test Data Bit 47
..	..	
..	..	
0	Read/write	Input Fifo Test Data Bit 40

after power up: 0x00000000

8.12.4 Test register 4 for Input FIFO Test (0x21C)

Bit	Read/Write access	Function
31	Read only	No function ; read “0”
..	..	
..	..	
8	Read only	No function ; read “0”
7	Read/write	Input Fifo Test Data Bit 39
..	..	
..	..	
0	Read/write	Input Fifo Test Data Bit 32

after power up: 0x00000000

8.13 Input Buffer Group 1 registers (0x220, 0x224, 0x228, 0x22C)

The status of the 64 inputs can be read in groups of 8-bit through the four input buffer group 1 and the four input buffer group 2 (read only) registers for test purposes.

8.13.1 Input Buffer 1 (0x220)

Bit	Read/Write access	Function
31	Read only	No function ; read “0”
..	..	
..	..	
8	Read only	No function ; read “0”
7	Read only	Input Buffer Data Bit 63
..	..	
..	..	
0	Read only	Input Buffer Data Bit 56

8.13.2 Input Buffer 2 (0x224)

Bit	Read/Write access	Function
31	Read only	No function ; read “0”
..	..	
..	..	
8	Read only	No function ; read “0”
7	Read only	Input Buffer Data Bit 55
..	..	
..	..	
0	Read only	Input Buffer Data Bit 48

8.13.3 Input Buffer 3 (0x228)

Bit	Read/Write access	Function
31	Read only	No function ; read “0”
..	..	
..	..	
8	Read only	No function ; read “0”
7	Read only	Input Buffer Data Bit 47
..	..	
..	..	
0	Read only	Input Buffer Data Bit 40

8.13.4 Input Buffer 4 (0x22C)

Bit	Read/Write access	Function
31	Read only	No function ; read “0”
..	..	
..	..	
8	Read only	No function ; read “0”
7	Read only	Input Buffer Data Bit 39
..	..	
..	..	
0	Read only	Input Buffer Data Bit 32

8.14 Time Shadow Registers (0x230, 0x234, 0x238, 0x23C)

The 32-bit wide time stamp can be read trough the four (read only) time shadow registers. To avoid incorrect reading caused by toggling bits, it is recommended to freeze the time shadow register by setting bit 0 of the input group control register, to read the time from the four time shadow registers and to unfreeze the time shadow register by clearing bit 0 of the input group control register again.
The time shadow register is updated with every clock tick as long as bit 0 of the input group control register is cleared.

8.14.1 Time Shadow Register 1; (0x230)

Bit	Function
31	No function ; read “0”
..	
..	
8	No function ; read “0”
7	Time Shadow Register Bit 31
..	
..	
0	Time Shadow Register Bit 24

8.14.2 Time Shadow Register 2 (0x234)

Bit	Function
31	No function ; read “0”
..	
..	
8	No function ; read “0”
7	Time Shadow Register Bit 23
..	
..	
0	Time Shadow Register Bit 16

8.14.3 Time Shadow Register 3 (0x238)

Bit	Function
31	No function ; read “0”
..	
..	
8	No function ; read “0”
7	Time Shadow Register Bit 15
..	
..	
0	Time Shadow Register Bit 8

8.14.4 Time Shadow Register 4 (0x23C)

Bit	Function
31	No function ; read “0”
..	
..	
8	No function ; read “0”
7	Time Shadow Register Bit 7
..	
..	
0	Time Shadow Register Bit 0

8.15 Input inversion group 2 register (0x204)

After power up the SIS3400 CDMS II latches leading edge transitions as “1”. Trailing edges can be selected for input channels 32 to 1 by setting bit 0 of this register.

Bit	Read/Write access	Function
31	read only	No function; read as 0
..	..	
..	..	
8	read only	No function; read as 0
7	read/write	reserved, read as 0
6	read/write	reserved, read as 0
5	read/write	reserved, read as 0
4	read/write	reserved, read as 0
3	read/write	reserved, read as 0
2	read/write	reserved, read as 0
1	read/write	reserved, read as 0
0	read/write	Input group 1 (channels 32:1) inversion mode

The power up reading is: 0x00000000

8.16 Input Group 2 FIFO test registers (0x310, 0x314, 0x318, 0x31C)

8.16.1 Test register 5 for Input FIFO Test (0x310)

Bit	Read/Write access	Function
31	Read only	No function ; read “0”
..	..	
..	..	
8	Read only	No function ; read “0”
7	Read/write	Input Fifo Test Data Bit 31
..	..	
..	..	
0	Read/write	Input Fifo Test Data Bit 24

after power up: 0x00000000

8.16.2 Test register 6 for Input FIFO Test (0x314)

Bit	Read/Write access	Function
31	Read only	No function ; read “0”
..	..	
..	..	
8	Read only	No function ; read “0”
7	Read/write	Input Fifo Test Data Bit 23
..	..	
..	..	
0	Read/write	Input Fifo Test Data Bit 16

after power up: 0x00000000

8.16.3 Test register 7 for Input FIFO Test (0x318)

Bit	Read/Write access	Function
31	Read only	No function ; read “0”
..	..	
..	..	
8	Read only	No function ; read “0”
7	Read/write	Input Fifo Test Data Bit 15
..	..	
..	..	
0	Read/write	Input Fifo Test Data Bit 8

after power up: 0x00000000

8.16.4 Test register 8 for Input FIFO Test (0x31C)

Bit	Read/Write access	Function
31	Read only	No function ; read “0”
..	..	
..	..	
8	Read only	No function ; read “0”
7	Read/write	Input Fifo Test Data Bit 7
..	..	
..	..	
0	Read/write	Input Fifo Test Data Bit 0

after power up: 0x00000000

8.17 Input Buffer Group 2 registers (0x320, 0x324, 0x328, 0x32C)

8.17.1 Input Buffer 5 (0x320)

Bit	Read/Write access	Function
31	Read only	No function ; read “0”
..	..	
..	..	
8	Read only	No function ; read “0”
7	Read only	Input Buffer Data Bit 31
..	..	
..	..	
0	Read only	Input Buffer Data Bit 24

8.17.2 Input Buffer 6 (0x324)

Bit	Read/Write access	Function
31	Read only	No function ; read “0”
..	..	
..	..	
8	Read only	No function ; read “0”
7	Read only	Input Buffer Data Bit 23
..	..	
..	..	
0	Read only	Input Buffer Data Bit 16

8.17.3 Input Buffer 7 (0x328)

Bit	Read/Write access	Function
31	Read only	No function ; read “0”
..	..	
..	..	
8	Read only	No function ; read “0”
7	Read only	Input Buffer Data Bit 15
..	..	
..	..	
0	Read only	Input Buffer Data Bit 8

8.17.4 Input Buffer 8 (0x32C)

Bit	Read/Write access	Function
31	Read only	No function ; read “0”
..	..	
..	..	
8	Read only	No function ; read “0”
7	Read only	Input Buffer Data Bit 7
..	..	
..	..	
0	Read only	Input Buffer Data Bit 0

8.18 Output FIFO (0x8000-0xFFFC or 0x10000 to 0x1FFFC)

The address range of the output FIFO (First In First Out) depends on the addressing mode.

Mode	FIFO Address range
A24	0x8000-0x8FFFC
A32	0x10000-0x1FFFC

The output FIFO consists of two 64Kx18-bit FIFO chips, which are used in parallel to hold the formatted 32-bit wide output word. Normally one address to read from would be sufficient for the FIFO, but as most VME masters use address auto increment on block transfers, a contiguous address block allows for more efficient readout. The address range was chosen in a fashion, that allows for the readout of half of the FIFO in one block read (which typically consists of many 256 Byte reads on the VME bus) if A32 addressing is used. Hence A32 is the preferred addressing mode in high speed readout applications.
The data format of the output FIFO data is described in section 10.

Note: read access to the empty output FIFO results in a bus error (BERR)

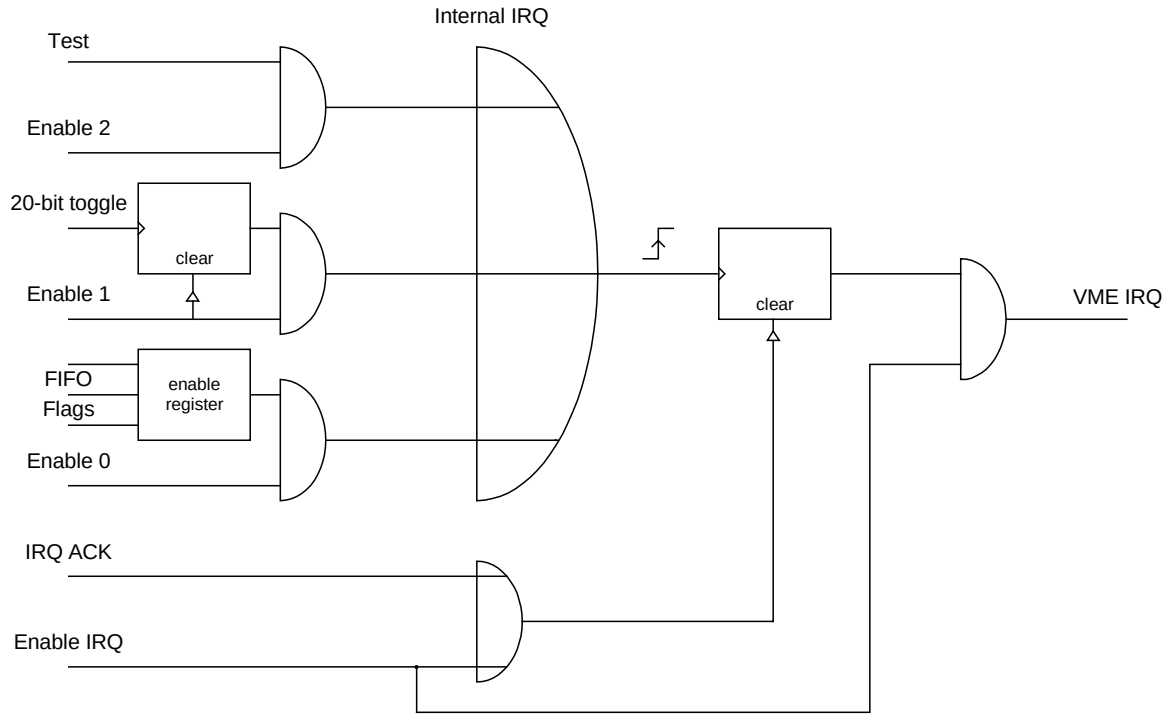
9 VME Interrupts

Three VME interrupt sources are implemented in the SIS3400 firmware design:

- output FIFO flag
- 20-bit counter roll over
- test

For compatibility with the LINUX Universe driver, the interrupts were implemented in release on acknowledge (ROAK) style .
Interrupt generation has to be enabled by setting bit 11 in the IRQ and version register. The internal VME interrupt flag can be used to check on an IRQ condition without actually making use of interrupts on the bus.
The VME interrupt level (1-7) are defined by bits 8 through 10 and the VME interrupt vector (0-255) by bits 0 through 7 of the VME IRQ and version register.

Find a diagram with the overall interrupt mechanism of the SIS3400 below



10 Data Format

At present two formatter data formats are implemented, the so called single wire mode and the so called event mode. In single wire mode **two** 32-bit words per hit (i.e. bit change 0→1) are written to the output FIFO .
The new status of all 64 input bits is written to the output FIFO in multi wire mode. Two more 32-bit words are needed to hold time and module Id. information.
Note: The output FIFO can be read in D32, BLT32 and MBLT32

10.1 Single Wire mode

32-bit word	bit 31	bits 30-26	bits 25-20	bits 19-0
1	Trailing (always 1)	Module Id.	Channel	0
2	Time Stamp (31-0)			

10.2 Multiwire mode

32-bit word	bit 31	bits 30-26	bits 25-20	bits 19-0
1	0	Module Id.	0	0
2	Time Stamp (bits 31-0)			
3	Input Bits 63-32 (channels 64-33) (bits 31-0)			
4	Input Bits 31-0 (channels 32-1) (bits 31-0)			

11 Input Configuration

SIS3400 CDMS II boards can be configured for TTL control levels with 50 Ohm or high impedance input termination and 100 Ohm or high impedance (resistor networks removed, recommended for daisy chaining only) RS485 inputs . The resistor networks are in sockets. For low active input levels the signals can be connected to V_{CC} through RN1B to RN18B with 1 KΩ.

Network	Channels
RN1A	Control Input 1
RN1B	Control Input 2
RN1C	Control Input 3
RN5A, 5B, 6A, 6B	1,2 3,4 5,6 7,8
RN7A, 7B, 8A, 8B	9,10 11,12 13,14 15,16
RN9A, 9B, 10A, 10B	17,18 19,20 21,22 23,24
RN11A, 11B, 12A, 12B	25,26 27,28 29,30 31,32
RN13A, 13B, 14A, 14B	33,34 35,36 37,38 39,40
RN15A,15B, 16A, 16B	41,42 43,44 45,46 47,48
RN17A, 17B, 18A, 18B	49,50 51,52 53,54 55,56
RN19A, 19B, 20A, 20B	57,58 59,60 61,62 63,64

12 Connector Specification

The two different types of front panel and VME connectors used on the SIS3400 CDMS II are:

Connector	Purpose	Part Number
160 pin zabcd	VME P1/P2	Harting 02 01 160 2101
LEMO00	Control in/output	LEMO EPB.00.250.NTN
68-pin	Input	Thomas&Betts HFR068RA29JSI

13 Signal Specification

13.1 Control Signals

The width of the start and stop pulse has to be greater or equal 15 ns, the maximum external clock shall not exceed **10 MHz**, the wave form has to be symmetric.

13.2 Inputs

The SIS3400 control section is designed for high active TTL inputs, by default the module is shipped with 50 Ohm input termination.

Logic Level	Level in V
0	< 0,8
1	> 2,4

The forbidden range between the high and low level can result in undefined states.
If 1K input termination is chosen, open inputs will be seen as “1”, control input inversion can be used to redefine them as “0”.
SIS3400 CDMS II inputs are designed for RS485 levels, the receiver input sensitivity is +/- 200 mV (refer to www.rs485.com for details). .

14 Operating Conditions

14.1 Power Consumption/Voltage requirement

To allow for the use of the SIS3400 independent of the users VME crate no non standard voltage is used by the board. In especial the card is a single supply (+5 V) design. The +3.3 V supply voltage for the on board FPGAs is generated by linear regulators. The actual power consumption of the module will vary with input data rate and may also depend on the actual firmware.

Operating conditions	Voltage in V	Current in A
SIS3400 Idle	+5	2,2
SIS3400-Clock 20 MHz	+5	
SIS3400 CDMSII Idle	+5	2,4

14.2 Cooling

Forced air flow is required for the operation of the SIS3400 board.

14.3 Insertion/Removal

Please note, that the VME standard does not support live insertion (hot swap). Hence crate power has to be turned off for installation and removal of SIS3400s in standard VME crates.
The leading pins on the SIS3400 VME64x VME connectors and connected on board circuitry are designed for hot swap in conjunction with a VME64x backplane (a VME64x backplane can be recognised by the 5 row VME connectors, while the standard VME backplane has three row connectors only).

15 Test

The SIS3400 provides a number of test features, which allow for debugging of the unit as well as for overall system setup tests.

15.1 LED (selftest)

During power up self test and LCA configuration all LEDs except the Ready (R) LED are on. After the initialisation phase is completed, all LEDs except the Ready (R), Power (P) and Disable (DIS) LED have to go off. Differing behaviour indicates either a problem with the download of the firmware boot file or one or more LCA and/or the download logic.

15.2 FIFO tests

15.2.1 Input FIFO test

Defined input data can be written to the input FIFO chips from VME when input mode 3 is selected via the control register. The data have to be written to the 8 input group 1/group 2 FIFO test registers and are transferred to the input FIFO chips upon a key address access to 0x38.(input control clock pulse).

15.2.2 Output FIFO test

The output FIFO chips can be tested in the same fashion as the input FIFO. Data are clocked into the output FIFO chips with a key address cycle to address 0x120 from the upper and lower output FIFO test registers. The test mode is enabled when input control mode 3 is activated.

16 Software Support

The first application of the SIS3400 was the FRM II TOF spectrometer readout system. A readout program with external configuration was developed for Dr. Jürgen Hannappels Universe II driver. The SBS-OR VP7 VME PC was used as platform, the driver has been tested with other Tundra Universe II based VME PCs also.
The latest CDMS II firmware version was tested with a PC and the SIS1100/3100 PCI to VME interface under LINUX.
The software for both systems will be provided on request by email or on disk. In addition the LINUX PCI to VME interface code will work with minimum modifications with the Windows 2000 driver for the SIS1100/3100 interface also..

17 Appendix

17.1 Address Modifier Overview

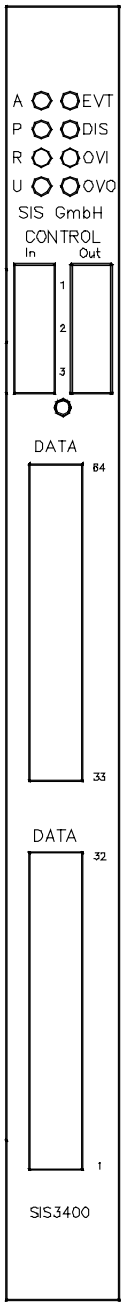
Find below the table of address modifiers, which can be used with the SIS3400 (with the corresponding addressing mode enabled).

AM code	Mode
0x3F	A24 supervisory block transfer (BLT)
0x3D	A24 supervisory data access
0x3C	A24 supervisory 64-bit block transfer (MBLT)
0x3B	A24 non-privileged block transfer (BLT)
0x39	A24 non-privileged data access
0x38	A24 non-privileged 64-bit block transfer (MBLT)
0x0F	A32 supervisory block transfer (BLT)
0x0D	A32 supervisory data access
0x0C	A32 supervisory 64-bit block transfer (MBLT)
0x0B	A32 non-privileged block transfer (BLT)
0x09	A32 non privileged data access
0x08	A32 non privileged 64-bit block transfer (MBLT)

17.2 Front Panel Layout

The front panel of the SIS3400 CDMS II is equipped with 8 LEDs, 6 control in- and outputs and 64 inputs. The control connectors are of LEMO00 style, the two input connectors are of 68-pin SCSI -style . The units are 4 TE (one VME slot) wide, the front panel is of EMC shielding type. VME64x/VIPA extractor handles are available on request or can be retrofitted by the user, if he wants to change to a VME64x/VIPA crate at a later point in time.
In the drawing below you can find the front panel layout.

Note: Only the aluminium portion without the extractor handle mounting fixtures is shown



17.3 List of Jumpers and Switches

Find below a list of jumpers and switches.

Name	Type	Function
J1	Array	Addressing mode selection
J34	Array	Boot mode selection
SW1	Rotary	Base address setting
SW2	Rotary	Base address setting

17.3.1 J1 Addressing Mode Selection

As described in section 7.2, the SIS3400 supports several addressing modes, the actual mode is selected by jumper array J1. The given mode is selected if ist corresponding jumper is in place. The four jumper positions are described in the table below.

Jumper	Function	Factory default
A32	enable A32 addressing	closed
A24	enable A32 addressing	closed
GEO	enable geographical addressing	open
VIPA	not implemented yet	open

Note: It is possible to have A32 and A24 set in parallel. If an A32 cycle is detected in this case, the setting of SW1 and SW2 is compared with A31-A24, if an A24 cycle is detected, SW1 and SW2 are compared with A23-A16.

17.3.2 J34 Boot Mode and File Selection

The firmware of the SIS3400 can be loaded off a FLASHPROM or via JTAG. In FLASHPROM boot mode up to four different boot files can be selected with the possible combinations of jumpers M3 and M4.

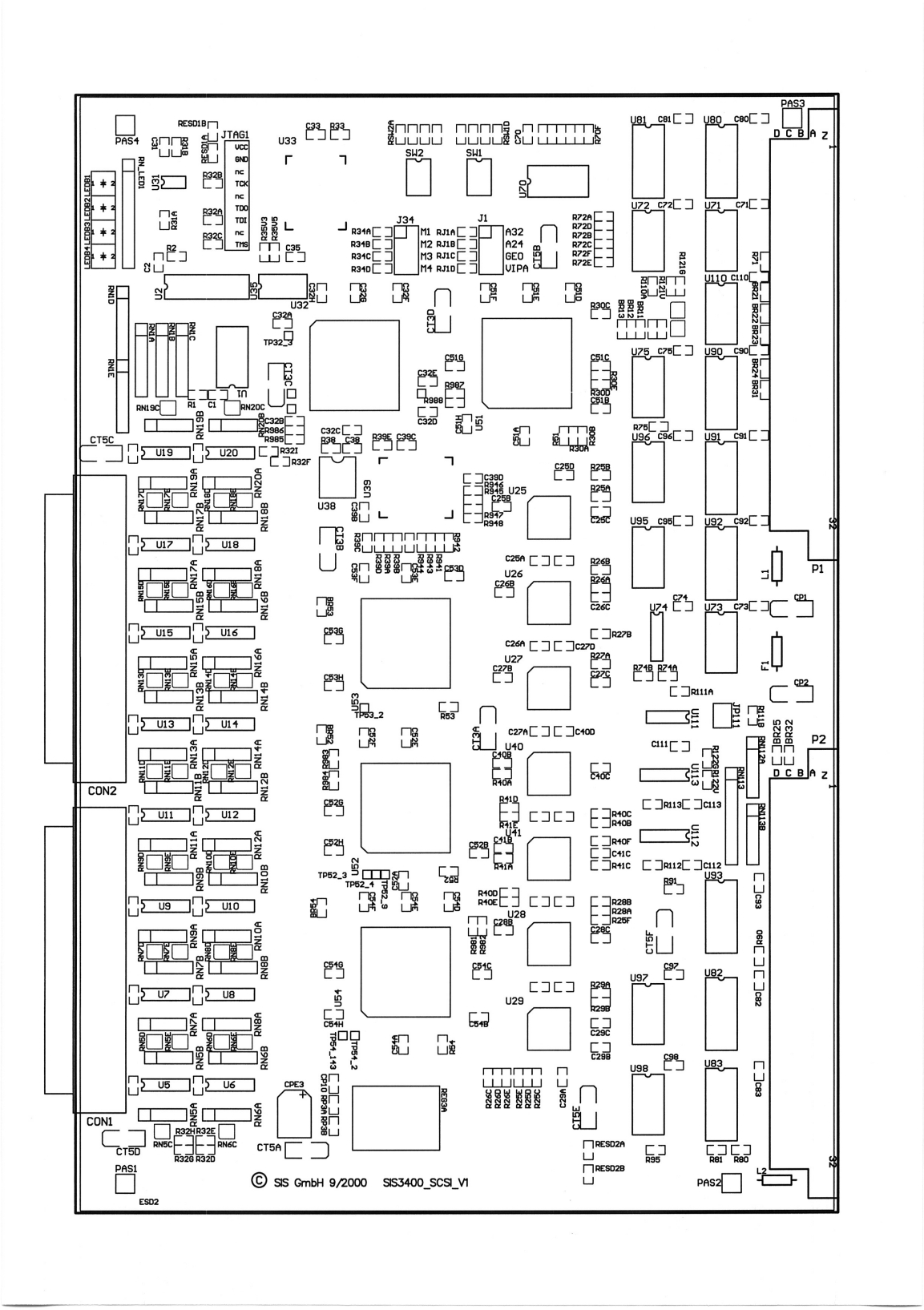
Jumper	Function	Factory default
M1	Reserved	closed
M2	Boot mode selection (closed FLASH, open JTAG)	closed
M3	Boot file Bit0 (closed = 0, open =1)	closed
M4	Boot file Bit1 (closed = 0, open =1)	closed

Note: The factory default setting (M2, M3 and M4 closed) boots file 0 from the FLASHPROM. For the SIS3400 clock distribution firmware the setting is M2 closed, M3 open, M4 closed (boot file 1 from FLASH).

17.3.3 SW1 and SW2 Base Address Selection

The two hexadecimal rotary switches SW1 and SW2 are used to define the VME base address in systems without geographical addressing capabilities (i.e. if standard VME crates are used). The two switches are labelled ADR_LO (SW1) and ADR_UP (SW2), as they define the lower and upper address nibble of the eight leading address bits (A31 to A24 with A32 enabled and addressed, A23 to A16 with A24 enabled and addressed). The setting of the two switches is ignored if a geographical addressing mode (GEO or VIPA) is enabled.

17.4 Board Layout



17.5 FLASHPROM Versions

A list of available FLASHPROMs can be obtained from http://www.struck.de/sis3400firm.htm. Please note, that a special hardware configuration may be necessary for the firmware design of interest.
The table on the web is of the format shown below:

SIS3400 FLASHPROM table

Design Name	Design	Boot File (s)
SIS3400_020300	0	SIS3400 Version 1
SIS3400_200400	0	SIS3400 Version 2 (clock module)
SIS3400_271000	0	SIS3400 Version 9 (CDMS II)
SIS3400_070501	0	SIS3400 Version 0xA (CDMS II)
SIS3400_200302	0	SIS3400 Version 0xB (CDMS II)

17.6 Row d and z Pin Assignments

The SIS3400 is ready for the use with VME64x and VME64xP backplanes. Features include geographical addressing and live insertion (hot swap). The prepared/used pins on the d and z rows of the P1 and P2 connectors are listed below.

Position	P1/J1		P2/J2	
	Row z	Row d	Row z	Row d
1		VPC (1)		
2	GND	GND (1)	GND	
3				
4	GND		GND	
5				
6	GND		GND	
7				
8	GND		GND	
9		GAP*		
10	GND	GA0*	GND	
11	RESP*	GA1*		
12	GND		GND	
13		GA2*		
14	GND		GND	
15		GA3*		
16	GND		GND	
17		GA4*		
18	GND		GND	
19				
20	GND		GND	
21				
22	GND		GND	
23				
24	GND		GND	
25				
26	GND		GND	
27				
28	GND		GND	
29				
30	GND		GND	
31		GND (1)		GND (1)
32	GND	VPC (1)	GND	VPC (1)

Note: Pins designated with (1) are so called MFBL (mate first-break last) pins on the installed 160 pin connectors, VPC(1) pins are connected via inductors.

17.7 Geographical Address Pin Assignments

The SIS3400 board can be used with geographical addressing via the geographical address pins GA0*, GA1*, GA2*, GA3*, GA4* and GAP*. The address pins are left open or tied to ground by the backplane as listed in the following table:

Slot Number	GAP* Pin	GA4* Pin	GA3* Pin	GA2* Pin	GA1* Pin	GA0* Pin
1	Open	Open	Open	Open	Open	GND
2	Open	Open	Open	Open	GND	Open
3	GND	Open	Open	Open	GND	GND
4	Open	Open	Open	GND	Open	Open
5	GND	Open	Open	GND	Open	GND
6	GND	Open	Open	GND	GND	Open
7	Open	Open	Open	GND	GND	GND
8	Open	Open	GND	Open	Open	Open
9	GND	Open	GND	Open	Open	GND
10	GND	Open	GND	Open	GND	Open
11	Open	Open	GND	Open	GND	GND
12	GND	Open	GND	GND	Open	Open
13	Open	Open	GND	GND	Open	GND
14	Open	Open	GND	GND	GND	Open
15	GND	Open	GND	GND	GND	GND
16	Open	GND	Open	Open	Open	Open
17	GND	GND	Open	Open	Open	GND
18	GND	GND	Open	Open	GND	Open
19	Open	GND	Open	Open	GND	GND
20	GND	GND	Open	GND	Open	Open
21	Open	GND	Open	GND	Open	GND

17.8 Additional Information on VME

The VME bus has become a popular platform for many realtime applications over the last decade. Information on VME can be obtained in printed form, via the web or from newsgroups. Among the sources are the VMEbus handbook, http://www.vita.com (the home page of the VME international trade association (VITA)) and comp.bus.arch.vmebus. In addition you will find useful links on many high energy physics labs web pages like CERN or FNAL

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